PATENT
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In Application of:	)	
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Seung Ho CHANG	)	
	)	Group Art Unit: Unknown
Application No.: To be assigned	)	
	)	
	)	Examiner: Unknown
Filed: Concurrently herewith	)	
	)	
For: METHOD OF PROGRAMMING/ READING MULTI-LEVEL FLASH MEMORY USING SENSING CIRCUIT	)	

Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the examination of the above-identified application, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claims 1-13, with the following:

1.(Amended) A method of programming a multi-level flash memory using a sensing circuit that includes a comparator, a reference current supply unit, a sense amplifier driving determining circuit, and a register array, the method comprising:

a data storing step of storing data, in a register, corresponding to a level to be programmed;

a second level program step of, after a first program voltage is applied to word lines, turning off the sensing circuit to maintain a threshold voltage at a first level voltage when the data stored in the register is a first memory cell being a first data, and performing a program to raise the threshold voltage to a second level when the data stored in the register is a remaining memory cells is other than the first data;

a third level program step of, after a second program voltage is applied to the word lines, turning off the sensing circuit to maintain the threshold voltage when the data stored in the register is one of the first being the first data and a second memory cell being a second data, and performing a program to raise the threshold voltage to a third level when the data stored in the register is a remaining memory cells is other than one of the first and second data; and

a fourth level program step of, after a third program voltage is applied to the word lines, turning off the sensing circuit to maintain the threshold voltage when the data stored in the register is one of the first memory cell being the first data, the second memory cell being the second data, and a third memory cell being a third data, and performing a program to raise the threshold voltage to a

fourth level when the data stored in the register is a remaining memory cells is other than one of the first data, the second data, and the third data.

2.(Amended) The method according to claim 1, wherein the first data is "11," the second data is "10," the third data is "01," and the fourth data is "00."

3.(Amended) The method according to claim 1, wherein the register includes a number of bits that represent all numbers of levels by which the memory cells can be programmed so that data on the level to be programmed is stored.

4.(Amended) The method according to claim 1, wherein the sensing circuit is turned OFF and ON by the sense amplifier driving determining circuit depending on the first to fourth data stored in the register.

5.(Amended) The method according to claim 1, further including an automatic verification program method, wherein an operation of the automatic verification program method is stopped at a time when the threshold voltage of the memory cells becomes higher than a reference cell of the reference current supply unit by comparing a reference current generated in the reference current supply unit with a drain current of the memory cells using the comparator.

6.(Amended) The method according to claim 1, wherein the first to third program voltages applied to the word lines are a medium voltage of each of the threshold voltages, and are sequentially applied from a low voltage.

7.(Amended) A method of reading a multi-level flash memory using a sensing circuit that includes a comparator, a voltage regulating block, a reference current supply unit, a sense amplifier driving determining circuit, a register array, and a counter, the method comprising:

a first initialization step of setting to store a fourth data in a plurality of registers, apply a first read voltage to word lines, and output a first data to the counter;

a first read step of sequentially comparing a first reference current of the reference current supply unit with a drain current of a plurality of memory cells in the comparator, and then storing a first data at a corresponding register to define a first memory cell when a threshold voltage is lower than a reference cell, and maintaining the fourth data stored in the register to complete a read operation of the first memory cell when the threshold voltage is lower than the reference cell;

a second initialization step of setting to apply a second read voltage to the word lines, and to allow the counter to output a second data;

a second read step of sequentially comparing a second reference current of the reference current supply unit with a drain current of the plurality of memory cells in the comparator only when the first memory cell is not read, and then

storing the second data at a corresponding register to define a second memory cell when the threshold voltage is lower than the reference cell, and maintaining the fourth data stored in the register to complete the read operation of the second memory cell when the threshold voltage is lower than the reference cell;

a third initialization step of setting to apply a third read voltage to the word lines, and to allow the counter to output a third data; and

a third read step of sequentially comparing a third reference current of the reference current supply unit with a drain current of the plurality of memory cells in the comparator only when one of the first and second memory cells is not read, and then storing the third data at a corresponding register to define a third memory cell when the threshold voltage is lower than the reference cell, and maintaining the fourth data stored in the register to complete the read operation of the third and fourth memory cells when the threshold voltage is lower than the reference cell.

8.(Amended) The method according to claim 7, wherein the register includes a number of bits that represent all numbers of levels by which the memory cells can be programmed to allow more than 2 bits to be stored when data in the multi-bit flash memory cell is more than 2 bits.

9.(Amended) The method according to claim 7, wherein the sense amplifier driving determining circuit determines whether the sensing circuit has to be driven depending on the data stored in the register.

10.(Amended) The method according to claim 7, wherein the first to third read voltages applied to the word lines are sequentially applied from a low voltage, and each correspond to a medium voltage of the threshold voltage levels.

11.(Amended) The method according to claim 7, wherein the first data is "11," the second data is "10," the third data is "01," and the fourth data is "00."

12.(Amended) The method according to claim 7, wherein the third read step detects only data of upper bits among data stored in the register, and then determines them to be one of the first and second memory cell when the data of upper bits is "1" to be remaining cells when the data of upper bits is "0."

13.(Amended) The method according to claim 7, wherein the sensing circuit is turned OFF and ON by the sense amplifier driving determining circuit depending on the first to fourth data stored in the register.

Conclusion

The foregoing amendments are being made to place the application in condition for examination. A favorable action on the merits is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attachment is captioned "Version with markings to show changes made."

If there are any other fees due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully Submitted,

By: _____
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Dated: December 10, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1 has been amended as follows:

1.(Amended) A method of programming a multi-level flash memory using a sensing circuit~~[, which]~~ **that** includes a comparator, a reference current supply unit, a sense amplifier driving determining circuit, and a register array, **the method** comprising:

a data storing step of storing data, ~~[at]~~ **in** a register, corresponding to a level to be programmed;

a second level program step of, after a first program voltage is applied to word lines, turning off ~~[said]~~ **the** sensing circuit to maintain ~~[the]~~ **a** threshold voltage at a first level voltage ~~[if]~~ **when** the data stored ~~[at said]~~ **in the** register is a first memory cell being a first data, and performing a program to raise the threshold voltage to a second level ~~[if]~~ **when** the data stored ~~[at said]~~ **in the** register is ~~[the]~~ **a** remaining memory cells ~~[being not]~~ **is other than** the first data;

a third level program step of, after a second program voltage is applied to ~~[said]~~ **the** word lines, turning off ~~[said]~~ **the** sensing circuit to maintain the threshold voltage ~~[if]~~ **when** the data stored ~~[at said]~~ **in the** register is **one of** the first ~~[or second memory cell]~~ being the first ~~[or]~~ **data and a second memory cell being a** second data, and performing a program to raise the threshold voltage to a third level ~~[if]~~ **when** the data stored ~~[at said]~~ **in the** register is ~~[the]~~ **a** remaining memory cells ~~[being not]~~ **is other than one of** the first ~~[or]~~ **and** second data; and

a fourth level program step of, after a third program voltage is applied to ~~[said]~~ **the** word lines, turning off ~~[said]~~ **the** sensing circuit to maintain the threshold voltage ~~[if]~~ **when** the data stored ~~[at said]~~ **in the** register is **one of** the first~~[, second or third]~~ memory cell being the first~~[, second or]~~ **data, the second memory cell being the second data, and a third memory cell being a** third data, and performing a program to raise the threshold voltage to a fourth level ~~[if]~~ **when** the data stored ~~[at said]~~ **in the** register is ~~[the]~~ **a** remaining memory cells ~~[being not]~~ **is other than one of** the first~~[,]~~ **data, the** second ~~[or]~~ **data, and the** third data.

Claim 2 has been amended as follows:

2.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 1, wherein ~~[said]~~ **the** first data is ~~[" 11 ", said]~~**"11," the** second data is ~~[" 10", said]~~**"10," the** third data is ~~["0 1"]~~**"01,"** and ~~[said]~~ **the** fourth data is ~~["00".]~~**"00."**

Claim 3 has been amended as follows:

3.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 1, wherein ~~[said]~~ **the** register ~~[has so much as the]~~ **includes a** number of bits that ~~[can]~~ represent all ~~[the]~~ numbers of levels by which ~~[said]~~ **the** memory ~~[cell]~~ **cells** can be programmed~~[,]~~ so that data on the level to be programmed is stored.

Claim 4 has been amended as follows:

4.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 1, wherein ~~[said]~~ **the** sensing circuit is ~~[tamed on/off by said]~~ **turned OFF and ON by the** sense amplifier driving determining circuit depending on ~~[said]~~ **the** first **to** fourth data stored ~~[at said]~~ **in the** register.

Claim 5 has been amended as follows:

5.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 1, ~~[wherein the program of said memory is]~~ **further including** an automatic verification program method, wherein an operation of the automatic verification program method is stopped at ~~[the]~~ **a** time when the threshold voltage of ~~[said]~~ **the** memory ~~[cell]~~ **cells** becomes higher than ~~[the]~~ **a** reference cell of ~~[said]~~ **the** reference current supply unit by comparing ~~[the]~~ **a** reference current generated in ~~[said]~~ **the** reference current supply unit with a drain current of ~~[said]~~ **the** memory ~~[cell]~~ **cells** using ~~[said]~~ **the** comparator.

Claim 6 has been amended as follows:

6.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 1, wherein **the** first ~~[,]~~**to** third program voltages applied to ~~[said]~~ **the** word lines are ~~[determined to be]~~ a medium voltage of each of the threshold voltages, and are sequentially applied from a low voltage.

Claim 7 has been amended as follows:

7.(Amended) A method of reading a multi-level flash memory using a sensing circuit~~[, which]~~ **that** includes a comparator, a voltage regulating block, a reference current supply unit, a sense amplifier driving determining circuit, a register array, and a counter, **the method** comprising:

a first initialization step of setting to store a fourth data ~~[at all the]~~ **in a plurality of** registers, apply a first read voltage to word lines, and output a first data to ~~[said]~~ **the** counter;

a first read step of sequentially comparing a first reference current of ~~[said]~~ **the** reference current supply unit with a drain current of ~~[the]~~ **a plurality of** memory cells in ~~[said]~~ **the** comparator, and then storing ~~[the]~~ **a** first data at a corresponding register to define a first memory cell~~[, if said]~~ **when a** threshold voltage is lower than ~~[the]~~ **a** reference cell, and maintaining the fourth data stored ~~[at]~~ **in** the register to complete ~~[the]~~ **a** read operation of ~~[said]~~ **the** first memory cell~~[, if said]~~ **when the** threshold voltage is lower than the reference cell;

a second initialization step of setting to apply a second read voltage ~~[said]~~ **to the** word lines, and to allow ~~[said]~~ **the** counter to output a second data;

a second read step of sequentially comparing a second reference current of ~~[said]~~ **the** reference current supply unit with a drain current of the **plurality of** memory cells in ~~[said]~~ **the** comparator only when ~~[said]~~ **the** first memory cell is not **read**, and then storing the second data at a corresponding register to define a second memory cell~~[, if said]~~ **when the** threshold voltage is lower than the

reference cell, and maintaining the fourth data stored ~~[at]~~ **in** the register to complete the read operation of ~~[said]~~ **the** second memory cell~~[, if said]~~ **when the** threshold voltage is lower than the reference cell;

a third initialization step of setting to apply a third read voltage ~~[said]~~ **to the** word lines, and to allow ~~[said]~~ **the** counter to output a third data; and

a third read step of sequentially comparing a third reference current of ~~[said]~~ **the** reference current supply unit with a drain current of the **plurality of** memory cells in ~~[said]~~ **the** comparator only when ~~[said]~~ **one of the** first ~~[or]~~ **and** second memory ~~[cell]~~ **cells** is not **read**, and then storing the third data at a corresponding register to define a third memory cell~~[, if said]~~ **when the** threshold voltage is lower than the reference cell, and maintaining the fourth data stored ~~[at]~~ **in** the register to complete the read operation of ~~[said]~~ **the** third and fourth memory cells~~[, if said]~~ **when the** threshold voltage is lower than the reference cell.

Claim 8 has been amended as follows:

8.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 7, wherein ~~[said]~~ **the** register ~~[has so much as the]~~ **includes a** number of bits that ~~[can]~~ represent all ~~[the]~~ numbers of levels by which ~~[said]~~ **the** memory ~~[cell is]~~ **cells can be** programmed~~[, thus allowing]~~ **to allow** more than 2 bits to be stored ~~[in case that]~~ **when** data ~~[on]~~ **in** the multi-bit flash memory cell is more than 2 bits.

Claim 9 has been amended as follows:

9.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 7, wherein ~~[said]~~ **the** sense amplifier driving determining circuit determines whether ~~[said]~~ **the** sensing circuit has to be driven depending on the data stored ~~[at said]~~ **in the** register.

Claim 10 has been amended as follows:

10.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 7, wherein **the** first ~~[ ]~~**to** third **read** voltages applied to ~~[said]~~ **the** word lines are sequentially applied from a low voltage**,** and each correspond to a medium~~[.]~~ voltage of the threshold voltage levels.

Claim 11 has been amended as follows:

11.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 7, wherein ~~[said]~~ **the** first data is ~~["11", said]~~**"11," the** second data is ~~["10", said]~~**"10," the** third data is ~~["01"]~~**"01,"** and ~~[said]~~ **the** fourth data is ~~["00".]~~**"00."**

Claim 12 has been amended as follows:

12.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 7, wherein ~~[said]~~ **the** third read step detects only data of upper bits among data stored ~~[at said]~~ **in the** register**,** and then determines them to be

one of the first ~~[or]~~ **and** second memory cell ~~[if]~~ **when** the data of upper bits is ~~[1 (one)]~~**"1"** to be remaining cells ~~[if]~~ **when** the data of upper bits is ~~[0 (zero).]~~**"0."**

Claim 13 has been amended as follows:

13.(Amended) The method ~~[of programming a multi-level flash memory]~~ according to claim 7, wherein ~~[said]~~ **the** sensing circuit is turned ~~[on/off]~~ **OFF and ON** by ~~[sa id]~~ **the** sense amplifier driving determining circuit depending on ~~[said]~~ **the** first ~~[ ]~~**to** fourth data stored ~~[at said]~~ **in the** register.